Modeling Minority Carriers Related Capacitive Effects for Transient Substrate Currents in Smart Power ICs

Camillo Stefanucci, Pietro Buccella, Maher Kayal, and Jean-Michel Sallese

Abstract—This paper presents an extended model for transient and ac circuit-level simulation of minority carriers propagation through the substrate of smart power integrated circuits (ICs). A p-n junction and a diffusion resistor with capacitive components are proposed to efficiently simulate transient parasitic coupled currents in high-power stages. From a general chip layout, an equivalent substrate network including capacitive effects (junction and diffusion capacitances) can be extracted and parasitic bipolar transistor can be simulated for the first time in transient operation by circuit simulators once the minority carriers continuity conditions are satisfied. This paper shows simulation results of the implemented models in good agreement with those obtained from technology computer-aided-design. This implies that transient layout dependent mechanisms between high-voltage aggressor wells and low-voltage victims can be verified in early stages of IC design flow.

Index Terms—Bipolar transistors, minority carriers, power semiconductor devices, smart power integrated circuit (IC), substrate noise.

I. INTRODUCTION

AUTOMOTIVE applications are more and more requiring power devices on integrated circuit (IC) together with their low-power control blocks. This integration on a single chip leads in the last years to the development of a new category of ICs, the smart power ICs [1].

The main problem when combining low- and high-power stages on the same chip is the sharing of the same substrate where high-voltage transistors inject majority or minority carriers during circuit operation. This is due to the typical presence of inductive loads, which can cause forward biasing of p-n junctions during drain switching with the consequent triggering of parasitic bipolar junction transistors (BJTs). As a result, current paths driven by diffusion of electrons and holes in the substrate are collected somewhere else on the chip causing malfunctions. The detection of these parasitic substrate paths depends on the layout of smart power ICs and it is very challenging to detect them during the design process.

The presence of high-voltage devices asks for developing new tools and models for circuit simulators in order to predict destructive effect in early design stages and avoid costly redesigns. However, since minority carriers are those responsible for such effects, no SPICE model can be used for that purpose. The common trend [2]–[4] is to use technology computer-aided design (TCAD) software based on finite-element method to simulate high-voltage circuits. This approach has demonstrated to be accurate [5] but at the cost of simulation times in the range of hours and high computer resources when addressing circuits.

A novel model methodology has been proposed in [6] to consider the diffusion of minority carriers in circuit simulators. It consists in the representation of the substrate with an equivalent 3-D parasitic network made of special diodes and resistances. This allows to track 3-D couplings for a general circuit layout. To simulate substrate coupling and parasitic bipolar paths, an extension of the physical model of the diode and the substrate resistance has been developed to consider minority carriers diffusion. The parasitic network resulting from a meshing strategy of the substrate is able to efficiently simulate dc coupling for high-voltage devices, e.g., the below-ground condition of an H-bridge [7].

Nevertheless, there are still no models available to simulate transient and ac couplings between the same high-voltage structures with circuit simulators. Nowadays, the only possibility to deal with these simulations is with TCAD software, as demonstrated in [8]. This paper focuses on the extension of a junction-based model for the substrate couplings that allows ac and transient simulation within circuit simulators. This is done by adding relevant capacitive components that can be efficiently simulated using Kirchhoff’s laws trading TCAD accuracy with simulation time.

This paper is organized as follows. Section II describes the proposed model methodology to simulate propagation of minority carriers in SPICE-compatible tools with time dependent phenomena. The frequency-dependent components added to the model are detailed in Section III with the equivalent circuit implementation. Section IV validates the proposed equations for diodes and bipolar transistors through TCAD simulations, while in Section V N-wells transient coupling study is reported. Finally, the conclusion is given in Section VI.

II. MODELING MINORITY CARRIERS PROPAGATION

In classical substrate noise analysis of mixed-signal circuits, the substrate is represented by an equivalent network of doping dependent resistors and capacitances at p-n junctions.
boundaries [9] (Fig. 1). This is valid when the analysis of the substrate is limited to drift currents and without minority carriers, but the presence of a junction also implies diffusion currents with injection of electrons or holes. Therefore, the complete description of the substrate has to consider both drift and diffusion currents. For the diffusion of minority carriers, the proposed Swiss Federal Institute of Technology (EPFL) substrate model [6] replaces the standard substrate resistors with diffusion resistors and standard junction capacitance with diodes able to inject and collect minority carriers (Fig. 1). Connecting together a network of these devices both minority and majority carriers currents in the substrate can be simulated. This approach is compatible with standard circuit simulators because the physical equations are expressed in terms of equivalent voltage and currents relying on Kirchhoff’s laws.

To extend this approach to transient phenomena the nonstationary drift–diffusion model must be considered. In 1-D continuity equation for the electron concentration \( \hat{n}(x) \) (similar equations apply for holes) can be written as

\[
\frac{d}{dx} \left( q \mu(x) \hat{n}(x) \right) + qD \frac{d\hat{n}(x)}{dx} = qR(x) + q \frac{d\hat{n}(x)}{dt} \tag{1}
\]

where \( R(x) \) is the general recombination term, \( E(x) \) is the electric field, \( \mu \) and \( D \) are the mobility and diffusivity of minority carriers, respectively, and \( q \) is the elementary charge. The total time-dependent current \( J_{nx} \) of minority carriers is not conserved because of the presence of recombination and analytical solution in closed form cannot be obtained with a spatial-dependent electric field. However, (1) can be linearized between \( N \) discretized points corresponding to \( N \) electrical nodes of a parasitic substrate circuit.

Let us consider a point \( i \) in the substrate distant \( \Delta x_i \) from the next point \( i + 1 \) and \( \Delta x_{i-1} \) from the previous point \( i - 1 \). A central difference scheme can be used for the current of minority carriers [10], as reported in

\[
\frac{dJ_{nx_i}}{dx} \approx \frac{J_{nx_{i+\frac{1}{2}}} - J_{nx_{i-\frac{1}{2}}}}{\Delta x_i} = q \left( R_i + \frac{d\hat{n}_i}{dt} \right) \tag{2}
\]

The midpoints \( i \pm 1/2 \) are assumed to be exactly at half distance between the first neighbors. The corresponding currents can still be approximated with the following form:

\[
J_{nx_{i+\frac{1}{2}}} = q \mu_{i+\frac{1}{2}} \hat{n}_{i+\frac{1}{2}} \frac{\dot{V}_i - \dot{V}_{i+1}}{\Delta x_i} + qD_{i+\frac{1}{2}} \frac{\hat{n}_{i+\frac{1}{2}} - \hat{n}_i}{\Delta x_i} \tag{3}
\]

where the midpoint quantities \( \mu_{i+1/2}, D_{i+1/2}, \) and \( \hat{n}_{i+1/2} \) can be expressed in terms of space average. Substituting (3) in (2) the linearized form, (4), at the \( i \)th node is obtained

\[
\frac{D_{i+\frac{1}{2}}}{\Delta x_i} (\hat{n}_{i+1} - \hat{n}_i) = \frac{D_{i-\frac{1}{2}}}{\Delta x_{i-1}} (\hat{n}_i - \hat{n}_{i-1}) + \mu_{i+\frac{1}{2}} \frac{\hat{n}_{i+\frac{1}{2}} + \hat{n}_i}{2} E_{i+\frac{1}{2}} - \mu_{i-\frac{1}{2}} \frac{\hat{n}_i + \hat{n}_{i-1}}{2} E_{i-\frac{1}{2}}
\]

\[
= \frac{\Delta x_i}{2} R_i + \frac{\Delta x_{i-1}}{2} R_i + \frac{\Delta x_i}{2} \frac{d\hat{n}_i}{dt} + \frac{\Delta x_{i-1}}{2} \frac{d\hat{n}_{i-1}}{dt} \tag{4}
\]

Considering the excess carriers concentrations \( \hat{n} \) like voltages, the continuity equation can be interpreted as a conservation law of currents. From the linearized form the equivalent \( T \)-circuited shown in Fig. 2 can be easily drawn. In the circuit, there are four elements: 1) the apparent conductance \( G_d \) modeling the drop of minority carriers concentration along the diffusion path; 2) the apparent conductance \( G_c \) for the recombination proportional to the carrier concentration (in the simplest models it is a resistor); 3) the transconductance \( g_{nd} \) to model the drift effect due to the electric field; and 4) the apparent capacitance \( C_d \) to add the minority carriers propagation delay.

This circuit can be embedded with the addition of two terminals in resistors and diodes to simulate minority carriers propagation through the substrate. The result consists in four-terminal devices, where the additional voltages and currents are equivalent representation for the excess concentration of minority carriers \( V_{eq} \) and their gradient \( I_{eq} \). The proposed
through the substrate and an additional space-varying charge has to be considered. The diffusion charge can be computed as the integral of the excess charge distribution of minority carriers in the quasi-neutral regions of the junction ($Q_p$ in the $N$-side and $Q_n$ in the $P$-side)

$$Q_p = +q \int_{x_n}^{W_p} p_n(x) \, dx, \quad Q_n = -q \int_{-W_p}^{-x_p} n_p(x) \, dx \quad (6)$$

where $x_n, x_p$ are the coordinates of the space charge region, $W_n$ and $W_p$ are the physical length of $N$ and $P$ side, respectively, $n_p(x)$ is the excess distribution of electrons in $P$ side, and $p_n(x)$ is the excess distribution of holes in the $N$ side. For an arbitrary applied bias no analytical formula for the carriers distribution can be derived and the total diffusion capacitance given by $C_d(V) = dQ/dV$ cannot be implemented with a closed-form equation. The expression for $C_d(V)$ is possible only for total recombination of carriers at the physical boundaries ($p_j = 0, n_j = 0$) assuming low-injection distribution of carriers, which leads to an exponential voltage-dependent capacitance [11]. However, the voltage dependency of boundary conditions $p_j, n_j$ of minority carriers is not generally known especially when they are injected from several points across the chip.

For arbitrary boundary conditions, it is still possible to approximate the integral of (6) using the distributed substrate network of the proposed modeling methodology. Since the proposed model tracks the minority carriers space concentration at a general point $i$ with the added terminal voltage $V_{eq,i}$, the charge $Q_i = A \Delta x_i V_{eq,i}$ is also known. As shown in Fig. 3, this corresponds to approximate the integrals in (6) with the rectangle method, where the drop of minority carriers concentration is modeled by a conductance $G_d$. Connecting together different devices the equivalent voltages dependent on $p_j, n_j$ boundary conditions will be solved by the simulator and the value of the diffusion charges will be automatically computed. To track the time variation of these charges (i.e., the diffusion capacitance), it is sufficient to add the term $C_{d,i} = A \Delta x_i dV_{eq,i}/dt$ to each diffusion conductance $G_d$.

In Fig. 4, the implementation of $C_d$ is presented. The upper circuit represents the standard doping dependent substrate resistance (minority carriers modulate this resistance but this effect is negligible in low injection) with a small correction term $J_{bulk}$ for the diffusion of majority carriers [12]. Notice that this upper circuit does not implicitly include any

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**III. SUBSTRATE CAPACITIVE EFFECTS**

Since the proposed substrate modeling methodology is based on junctions, it is sufficient to analyze only diode’s capacitive components: the junction capacitance and the diffusion capacitance. While the first one is well modeled and already included in mixed-signal substrate tools, the second one lacks a proper model since it strongly depends on minority carriers concentration.

In the following sections, a charge-based model for these capacitances is presented for general minority carriers distribution at the terminals of p-n junctions. The total ac contribution of such capacitances can indeed be expressed as the time derivative of diffusion and depletion charges as in (5), where $A$ is the cross section area of the considered junction

$$I_{ac}(V) = A \frac{dQ_p}{dt} - A \frac{dQ_n}{dt} + A \frac{dQ_j}{dt}.$$  \quad (5)

The proposed implementation of these capacitive effects will be explained in terms of equivalent circuits for the distributed substrate network.

**A. Diffusion Capacitance**

The diffusion capacitance becomes dominant in forward bias condition, where there is an injection of minority carriers across a junction. These carriers diffuse, as sketched in Fig. 3,
capacitance. Capacitances are added only in the bottom minority carriers circuit and, as detailed in Section II, this is equivalent to a finite-difference discretization of the non-stationary drift–diffusion continuity equation. (Fig. 4 shows the Π network of the T-circuit in Fig. 2.) However, the two circuits are coupled in the overall substrate network such that the time variation of minority charges affects the real ac which propagates in the substrate. Notice that the presented implementation does not require any additional parameters in the model.

B. Junction Capacitance

The depletion charges in the space charge region of a diode represent the second nonlinear capacitive element. The depletion region width varies with the applied voltage in a nonlinear way depending on the doping profile around the junction. Hereafter, we consider a general space-dependent doping profile of the form \( x = 0 \) corresponds to the metallurgical junction

\[
N(x) = \begin{cases} 
D_1 x^{m-2}, & \text{for } x < 0 \\
D_2 x^{m-2}, & \text{for } x \geq 0 
\end{cases}
\]

(7)

with \( D_1, D_2 \) constant parameters, \( m = 2 \) for the abrupt case and \( m = 3 \) for the linear one. The well-known solution of Poisson’s equation considering neutrality and complete ionization leads to the following expression for the depletion region width in function on the junction potential drop \( V_J \) [14]:

\[
x_d(V_J) = \left( \frac{\varepsilon_s [V_{bi} - V_J]}{q} \right)^{\frac{1}{m}} \left( D_1^{-\frac{1}{m-1}} + D_2^{-\frac{1}{m-1}} \right)^{\frac{1}{m-1}}
\]

(8)

where \( V_{bi} \) is the built-in potential and \( \varepsilon_s \) is the dielectric permittivity of silicon. The corresponding junction capacitance \( C_J(V_J) \) is not dependent on the minority carriers boundary conditions, thus it is equivalent to the one of standard SPICE diode models and already included in mixed-signal substrate tools. The circuit implementation is then straightforward, but it is expressed in terms of a time-varying charge \( Q_J \). The expression \( Q_J(V_J) \) is given by (9) and has the advantage to not diverge for \( V_J \geq V_{bi} \) since it is related to the depletion width which rapidly tends to zero in forward bias. This avoids numerical problems in the implementation and no linearization is required as in SPICE diode models

\[
Q_J = \frac{q x_d^{m-1}}{(m-1) \left( D_1^{-\frac{1}{m-1}} + D_2^{-\frac{1}{m-1}} \right)^{m-1}}.
\]

(9)

In Fig. 5, the EPFL diode equivalent circuit with the implementation of \( C_J \) is reported. It is composed of the connection of a \( P \) and \( N \) resistance, where the current injected across the junction is modeled by a controlled current source dependent on minority carriers total current computed on the bottom minority carriers circuit (for details see [15]). In this circuit, the previously described diffusion capacitances are included and the injected concentration of holes \( V_{eq,n} \) in the \( N \)-side and of electrons \( V_{eq,p} \) in the \( P \)-side are modeled by controlled voltage sources, which are exponentially dependent on the voltage \( V_J \) across the junction [13]. Finally, the depletion capacitance \( C_J \) can be simply added as a nonlinear element in the top total current circuit between the \( N \) and \( P \) series resistances, as in classical substrate tools.

IV. Model Validation

The proposed model equations are coded in VerilogA and simulated in Cadence Spectre environment. The validation of the results has been done by comparing the circuit simulations with TCAD simulations using Synopsys Sentaurus software. The parameters in TCAD and in the VerilogA code are the same: geometrical ones (cross section area and lengths) and technological ones (doping concentration, built-in potential, junction grading coefficient, and carriers’ lifetime). Shafetter’s relations for doping dependent lifetimes [16] as well as Arora’s model for doping dependent mobility of electrons and holes are considered [17]. In the following, ac analyses are reported for a simple 1-D diode and a parasitic lateral bipolar transistor in a 50 V technology.

A. Diode Capacitance and Inductance

To verify the capacitances introduced in the model two abrupt p-n junctions are considered. For completeness N+ and P+ contacts of 500 nm are added at the extremities with a dopant concentration of around \( 10^{19} \text{ cm}^{-3} \). The two diodes have the \( N \)-side 5 \( \mu \text{m} \) width and differ only by the \( P \)-side length: the first is a short diode of \( W_p = 10 \mu \text{m} \) emulating the distance between a well and a \( P+ \) contact, while the second is a long diode with \( W_p = 500 \mu \text{m} \) emulating a wafer backside contact beneath a well. The doping of \( N \)-side is \( N_d = 10^{17} \text{ cm}^{-3} \), the one of \( P \)-side is \( N_p = 10^{16} \text{ cm}^{-3} \).

The simulated \( CV \) plot for the two different diodes is reported in Fig. 6. In reverse bias, the model simulates the junction capacitance as in standard SPICE models. In forward bias, the capacitive effects related to minority carriers drift–diffusion appears. At few hundreds of millivolts the exponential increase of the diffusion capacitance is present. However, the value of the capacitance reaches a maximum then decreases and becomes negative, i.e., like an inductance [18]. The diode’s inductive behavior can be explained as a consequence of the high-minority carriers injection and the induced spatially modulated conductivity [19]. Classical SPICE models can simulate this effect only by adding an extrinsic lumped inductance to the diode compact model. On the other hand, the model proposed in this paper is intrinsically able to predict such an inductive behavior since it includes delay in minority
carriers response. Unlike for the junction capacitance, the
diffusion capacitance is frequency dependent because of such
a delay. As a consequence the simulated impedance depends
on the diode length and due to the distributed nature of the
proposed approach, frequency variations up to 100 MHz are
correctly simulated.

Furthermore, the ac phase $\phi$ of the impedance is reported
in Fig. 7 for the short diode. Starting from a $-\pi/2$ phase-shift
typical of a capacitor in reverse bias and low injection, almost
zero phase is obtained in high injection. This means that the
parasitic inductance is small and the diode behaves more like
a resistor.

B. Bipolar Transistor Cutoff Frequency

The back-to-back and/or front-to-front connection of two
EPFL diodes is able to simulate the parasitic BJTs between
two wells with different base distances. Since all the capacitive
components are embedded in the diode, no extra base–emitter,
base–collector, or collector–emitter capacitances need to be
added to consider the frequency-dependent effects of a BJT.
To show that, a simple lateral parasitic BJT between two
$N$ wells in a low-doped $P$ substrate is considered. The
geometrical and technological parameters used are reported
in Fig. 8 with the corresponding equivalent circuit model.
The effects of the $N^+$, $P^+$ contacts on the minority carriers
propagation [20] are considered as well.

AC simulations have been performed by applying a signal
to the base–emitter junction with the collector reverse biased
at 50 V in the case the two wells are 20 $\mu$m distant. The
hybrid $|h_{21}|$ parameter variation in frequency is reported for
low-injection and high-injection case in Fig. 9. It can be
noticed that the model is well fitted with TCAD results and the
simulated current gain decreases for high frequencies reaching
0 dB at the cutoff frequency $f_T$. Repeating the simulation for
different dc bias, the variation of $f_T$ is reported in Fig. 10.
As known, $f_T$ has a maximum, and then decreases in high
current regimes due to the $\beta$ rolloff. It should be mentioned that the extraction of $f_T$ requires several ac simulations over a wide-frequency range. The time required to obtain 10 $f_T$ points in TCAD last around 4 h for this simple case, while only 9 min are required in circuit simulator for processing a greater number of points.

Moreover, the model is able to well predict the variation of $f_T$ on the base length. If indeed the distance between two $N$ wells is doubled, the delays related to minority carriers increases with the consequent reduction of the $f_T$ (Fig. 10). This means that different parasitic BJTs present in a given technology will have not only different gains but also different delay times which could be easily handled by the proposed SPICE-compatible model.

V. TRANSIENT COUPLING IN SMART POWER ICs

The model can be easily extended in 2-D and 3-D cases. For this purpose, we report the simulation results of the 2.5-D test structure of Fig. 11, where the overall depth is considered to be 150 $\mu$m. The example consists in a typical aggressor–victim configuration of smart power ICs where a high-voltage MOS drain (e.g., the output stage of an $H$-bridge) undergoes below-ground condition with the corresponding forward biasing of the $N$-well and injection of substrate current. Other low-voltage wells (e.g., biased at 5 V) act as current collectors even if distant from the aggressor, in this case >70 $\mu$m. The overall system is then a multicollector parasitic lateral BJT, where electrons drift-diffuse in the low-doped substrate ($N = 4 \cdot 10^{15} \text{ cm}^{-3}$), which acts as a distributed base kept at 0 V.

We performed transient TCAD simulations of this structure using Gaussian doping profiles for the $N$ wells ($N_{peak} = 2 \cdot 10^{17} \text{ cm}^{-3}$) and for the contact N+, P+ implantations ($N_{peak} = 5 \cdot 10^{19} \text{ cm}^{-3}$) maintaining lifetime and mobility doping dependences. Since the corresponding substrate circuit reported in Fig. 11 is based on average doping concentrations, a tuning of the input parameters for the EPFL substrate model has been done.

A transient stimulus is applied to the high-voltage well $N_1$ emulating an inductive load at the output of a power stage. A 50-$\mu$s constant current pulse $I_{N_1}$ is then used with a rise and falling time of 1 $\mu$s, which causes the well $N_1$ to be forward bias and the voltage $V_{N_1}$ to go below ground.

The simulation results are shown in Fig. 12 for two different configurations corresponding to different injection levels of minority carriers. In the first configuration, a current of 150 $\mu$A is injected into the substrate forcing $V_{N_1} = -0.67$ V. This current is mainly collected by the P+ contacts during the transient rise time, but after tens of microsecond (corresponding to the lifetime of minority carriers) the near wells $N_2, N_3$ are finally collecting most of the injected electrons. In particular, $N_1$ collects 59%, $N_2$ 27%, and the substrate only 14%.

In the second configuration, 150 mA of current are injected corresponding to $V_{N_1} = -1$ V. Now the P+ contacts collects 49% of the injected currents, also after 20 $\mu$s, while 52.5 mA flows through the nearest collector $N_2$ (35%) and only 24 mA to the farthest collector $N_3$ (16%). This means that depending on the level of minority carriers we can obtain very different results. The proposed model required only 5 s for this transient simulation and can be used by designers to investigate different ICs layout. In this example, it allowed to predict that in high-injection regimes the P+ contacts are more efficient to collect currents than in low-injection case.

For this simulation, the simulation time required for TCAD is around 15 s per time step, while for the circuit model...
obtain valuable results with a gain of simulation time of is only 10 ms per time step. As a consequence, we can obtain valuable results with a gain of simulation time of around 1000.

VI. CONCLUSION

As a matter of fact, the propagation of electrons and holes through the substrate represent a space- and time-varying charge, which has never been included in substrate tools. The space dependency can be simulated considering a parasitic substrate network which can be extracted for a generic IC layout and technology using two four-terminal devices, a diode, and a resistance, to consider minority carriers.

This paper presented a charge-based substrate model extension including capacitive effects related to these minority carriers. In the enhanced diode model, the junction capacitance covers the standard substrate noise capacitive model, while the enhanced diffusion resistance includes the minority carriers related nonlinear diffusion capacitances.

The distributed nature of the final parasitic networks inherently allows to track time dependent effects related to the injection of minority carriers through the substrate of a smart power ICs. The proposed SPICE-compatible model has been shown to efficiently simulate capacitive and inductive behavior of power diodes, \( f_T \) of bipolar transistors and transient coupling of multicollector bipolar when compared to TCAD simulation for different injection regimes of minority carriers.

For the first time transient simulations of parasitic couplings in smart power ICs can be performed within circuit simulators. By extension, the modeling methodology can be applied to a 3-D layout as well, and the model can help designers to simulate effects of parasitic currents during early design stages.

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